Test Vector Micro-Instructions, UUT Synchronization. Here is the test vector code to do a TX Descriptor Read

1. Wait for STE to issue a PCI request as the Initiator (STE asserts REQn Output Low on vector label Wait\_TX\_Desc\_REQ:).
2. The tester, which is now the Target, gives the STE its GNTn.
3. Wait up to 16 PCI Clocks on vector labeled Wait\_Memory\_Access\_1 to match the DUT response with its expected response—the STE issues the transmit descriptor base address 0x40000000 on the PCI AD bus and the Memory Read command (0x6) on the command bus, and asserts FRAME#.
4. Insert dummy turn-around per the Read Transaction waveform.
5. The target gives the STE Bus Master its DEVSELn and TRDYn by driving them to logic 0. The STE will then begin reading the TX Descriptor first of 4 D-Words TDES0 (pointed to by the transmit descriptor address) on the next PCI Klunk.

Note: the reading means the tester has to drive the TXDES0 one bit MSB 31 Hi. TRDYn is used to hold off the master until the target is ready. On the next the PCI Clock, the tester provides TXDES1 = x62000040

which sets the buffer size. 40= 0100 0000 sets the 2 byte count to 2\*\*6= 64 bytes. 64 bytes/4 bytes per

D-word= Burst Length of 16. On the next PCI Clock, TXDES2, which is the TX Buffer Address 0xA0000000, is written into (read by) the STE.