# Summary of FAST PINS Features

* Timing Generators: powerful clock management tiles (CMT), combining phase-locked loop (PLL) and mixed-mode clock manager (MMCM) blocks for high precision and low jitter.
* Integrated block for PCI Express® (PCIe), standard x1 Lane Gen 2 and up to x8 Gen3 Endpoint and Root Port designs. Includes easy-to-edit user-programmable synthesizable Traffic Generator.
* Test program source.
* [WinChar](#_Windows_Characterization_GUI) includes I/V curve tracer.
* User software suite includes vector fail Capture RAM; AC/DC parametrics datalogger and debug modes including Row and Columns Mask; graphical [SHMOO](#_SHMOO_GUI); and a JTAG device programmer/boundary scan unit.,
* The At-Spex 512-400 FAST PINS module architecture adds unprecedented small system capability in the following areas: At-Speed AC Functional Test Rate across all channels, Vector Depth, increased Pin Count, Hi Current User Power Supplies for fmax testing as well as preserving the original features of the acclaimed [LMO500’s AC/DC Precision Pins.](#_Legacy_LMO_Standard)
* Speed. True 400 MHz programmable vector rate.
* 13 ps edge resolution.
* Deep. Up to 1 Gig vector pattern depth.
* Wide. 512 tester I/O channels.
* Small. 250 MHz benchtop IC tester.
* Twelve Programmable DUT user power supplies DPS w/ Programmable Current Limiting: Four 8A and eight 2A HAPS -.6V to 6.5V, 24-bit dynamic range current measurement.
* Reconfigurable. User-selectable ASIC I/O pin levels: all 3.3V, 2.5V, 1.8V, 1.5V, 1.2V and 1V single-ended and differential standards.
* High throughput. Mainframe-competitive AC and DC parametric test times example 100 pin DUT w/ 25,000 vectors containing 4,000 transitions- 4 sec total to measure and datalog to a file. Time search algorithm averages 11 iterations to acquire an edge to 10 ps res.
* Self-test auto-verifies and datalogs all channels for functional Drive/Compare and AC/DC source and measure.
* Microprogrammable FPGA-based tester hardware now includes the vector processor unit (VPU), pin formatters, error logic and pipelines and DUT I/O. At-Spex IP includes 1066 MHz 1GB DDR3 DIMM Vector Memory Controller; 400 MHz Test Controller Gate Array PEG, Dual Pin 1.1 GBs Bipolar Pin Electronics switchable to CMOS Select I/O.
* Quick. Deep Vector Loads accomplished w/ Broadband to the Test Head.
* Built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology, 7 series FPGAs.
* Like a space satellite whose entire mission needs to be changed in mid-flight, the Pin Electronics Gate Array is reconfigurable via the test program.
* Modern enabling technologies: 28 nm 1156 pin, Stacked Silicon Interconnect SSI flip-chip fBGA FPGA’s w/ state of the art clock management; Embedded PCI Express SBC.

*This document describes the design architecture performance specifications of the Model 512-250, and is subject to change without notice.*